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ALGORITHM AND ARCHITECTURE FOR PRIME-FACTOR IDCT

1. **Dr.DeepikaPatnaik,** Faculty, Gandhi Institute of Engineering and TechonologyGunupur,Odisha,India
2. **Dr.S.S.Nayak,** Faculty, Centurion University of Technology and Management (JITMCampus), Paralakhemundi
3. **Dr. Banitamani Mallik,** Faculty, Centurion University of Technology and Management(JITMCampus),Paralakhemundi

Abstract

In this paper, we have suggested a simple scheme for prime-factor decomposition of Inverse Discrete Cosine Transform (IDCT) and systolic mesh architecture for its implementation. It is interesting to note that the transposition of the intermediate matrix is avoided in this structure by orthogonal processing during the pair of matrix multiplication i.e., if the processing for the first matrix multiplication takes place along X-direction, the processing for the second matrix multiplication is carried out along Y-direction. Due to this feature, the structure is highly compact, offers saving for transposition hardware and at the same time yields high throughput with less latency.

Keywords:

Inverse Discrete cosine Transform (IDCT), Prime-factor decomposition,VLSI, Systolic architecture, Orthogonal processing.

Author correspondence:

First Author,
Dr.DeepikaPatnaik, Faculty, Gandhi Institute of Engineering and TechonologyGunupur,Odisha,India

1. Introduction

The prime-factor decomposition technique is popularly used for fast computation of digital convolution and discrete orthogonal transforms. Prime-factor decomposition approach has, therefore, been tried for efficient computation of the DCT. The main theoretical rationale of this technique is to convert N-point DCT into a two dimensional ($N_1 \times N_2$)-point DCT by employing certain index mapping where $N = (N_1 \times N_2)$. Then we can deal with the resulting groups of small size problems in each dimension. In a DSP processor the memory for data storage is always expensive. By the prime-factor approach it is feasible to implement the long-length DCT by processor of small memory as short-length DCTs are implemented one after the other. In addition, when this approach is combined with efficient short-length algorithms the computational complexity is reduced considerably. Cho and Lee [2][1] derived prime-factor DCT algorithm based on various DFT algorithm which requires complex number multiplications. Yip and Wang [7][2] presented a prime factor decomposed algorithm for fast computation of DCT. Yang and Narasimha [6][3] proposed a prime-factor DCT algorithm which included only real-number multiplications. However, its index mapping was complicated. Lee [4][4] presented input and output index mapping for a prime-factor decomposed computation of DCT. However, his input index mapping is realized by constructing and combining two index tables, which occupy additional memory space and would be infeasible in variable-size applications. Chakrabarti and Ja`Ja` [1] developed a systolic architecture implementing

Lee's algorithm. They wanted to compute the DCT from DHT. So they modified the index mappings which are essentially the same as Lee's. However, they did not discuss the actual implementation of these index mappings. Lee and Huang [5] suggested scheme for prime-factor decomposition of the DCT which involves simpler and more efficient index mapping compared with those of [4, 6] and is devoid of complex arithmetic operations as well. Also they proposed two systolic architectures comprising of two matrix multiplication units and a transposition unit. In Section II, we have presented prime-factor decomposition of IDCT.

2. PRIME FACTOR DECOMPOSITION Of IDCT

The inverse discrete cosine transform (IDCT) may be written as

$$x(n) = \sum_{k=0}^{N-1} X(k) \cos[\pi(2n+1)k/2N] \quad (1)$$

when transform length $N = N_1 \times N_2$, N_1 and N_2being relatively prime.The input index k in equation (1) may be mapped into (k_1, k_2) as

$$k = (N_2k_1 + N_1k_2) \bmod N \quad (2)$$

For$N_2k_1 + N_1k_2 < N$,

Using equation (2) , equation (1) may be expressed as

$$x(n) = \sum_{k_1=0}^{N_1-1} \sum_{k_2=0}^{N_2-1} X(k_1,k_2) \cos\left[\frac{\pi(2n+1)(N_2k_1+N_1k_2)}{2N}\right] \quad (3)$$

$$= \sum_{k_1=0}^{N_1-1} \sum_{k_2=0}^{N_2-1} X(k_1,k_2) \cos\left[\frac{\pi(2n+1)k_1}{2N_1} + \frac{\pi(2n+1)k_2}{2N_2}\right] \quad (4)$$

$$= \sum_{k_1=0}^{N_1-1} \sum_{k_2=0}^{N_2-1} X(k_1,k_2) \cos\left[\frac{\pi(2n+1)k_1}{2N_1}\right] \cos\left[\frac{\pi(2n+1)k_2}{2N_2}\right] - X(k_1,k_2)\sin\left[\frac{\pi(2n+1)k_1}{2N_1}\right] \sin\left[\frac{\pi(2n+1)k_2}{2N_2}\right] \quad (5)$$

Equation(3) may otherwise be expressed as

$$x(n) = \sum_{k_1=0}^{N_1-1} \sum_{k_2=0}^{N_2-1} [X(k_1,k_2) - X(N_1-k_1, N_2-k_2)] \cos\left[\frac{\pi(2n+1)k_1}{2N_1}\right] \cos\left[\frac{\pi(2n+1)k_2}{2N_2}\right] \quad (6)$$

for $N_2k_1 + N_1k_2 > N$, equation (1) may be expressed as

$$x(n) = \sum_{k_1=0}^{N_1-1} \sum_{k_2=0}^{N_2-1} X(k_1,k_2) \cos\left[\frac{\pi(2n+1)(N_2k_1+N_1k_2-N)}{2N}\right] \quad (7)$$

$$= (-1)^n \sum_{k_1=0}^{N_1-1} \sum_{k_2=0}^{N_2-1} X(k_1,k_2) \sin\left[\frac{\pi(2n+1)k_1}{2N_1}\right] \cos\left[\frac{\pi(2n+1)k_2}{2N_2}\right] \quad (8)$$

$$= (-1)^n \sum_{k_1=0}^{N_1-1} \sum_{k_2=0}^{N_2-1} [X(k_1,k_2) \sin\left[\frac{\pi(2n+1)k_1}{2N_1}\right] \cos\left[\frac{\pi(2n+1)k_2}{2N_2}\right]$$
$$+X(k_1,k_2) \cos\left[\frac{\pi(2n+1)k_1}{2N_1}\right] \sin\left[\frac{\pi(2n+1)k_2}{2N_2}\right]] \quad (9)$$

$$=(-1)^n \sum_{k_1=0}^{N_1-1} \sum_{k_2=0}^{N_2-1} [X(N_1-k_1,k_2)(-1)^n$$
$$\cos\left[\frac{\pi(2n+1)k_1}{2N_1}\right] \cos\left[\frac{\pi(2n+1)k_2}{2N_2}\right]+$$
$$X(k_1,N_2-k_2)(-1)^n \cos\left[\frac{\pi(2n+1)k_1}{2N_1}\right] \cos\left[\frac{\pi(2n+1)k_2}{2N_2}\right] \quad (10)$$

$$x(n) = \sum_{k_1=0}^{N_1-1} \sum_{k_2=0}^{N_2-1} [X(N_1-k_1,k_2)+X(k_1,N_2-k_2)]$$
$$\cos\left[\frac{\pi(2n+1)k_1}{2N_1}\right] \cos\left[\frac{\pi(2n+1)k_2}{2N_2}\right] \quad (11)$$

Equation (6) and (11) may be expressed as

$$x(n) = \sum_{k_1=0}^{N_1-1} \sum_{k_2=0}^{N_2-1} y(k_1,k_2) \cos\left[\frac{\pi(2n+1)k_1}{2N_1}\right] \cos\left[\frac{\pi(2n+1)k_2}{2N_2}\right] \quad (12)$$

$y(k_1,k_2)= X(k_1,k_2) – X(N_1-k_1, N_2-k_2)$ for $N_2k_1+ N_1k_2<N$ and

$= X(N_1-k_1,k_2) + X(k_1, N_2-k_2)$ for $N_2k_1 + N_1k_2>N$ (13)

The output index n in equation (12) may be mapped into (n_1,n_2) as (Kung, S.Y.et.al)[8]

$$n_i = \begin{cases} \bar{n}_i & \text{if} \bar{n}_i < N_i \text{for i } = 1 \text{ and } 2 \\ 2N_i - 1 - \bar{n}_i & \text{otherwise where } \bar{n}_i = n \bmod 2N_i \end{cases} \quad (14)$$

Using equation (13) and (14), equation (12) can be written as

$$x(n_1,n_2)= \sum_{k_1=0}^{N_1-1} \sum_{k_2=0}^{N_2-1} y(k_1,k_2) \cos\left[\frac{\pi(2n_1+1)k_1}{2N_1}\right] \cos\left[\frac{\pi(2n_2+1)k_2}{2N_2}\right] \quad (15)$$

Due to orthogonal nature of the DCT , the forward transform, may however, be realised by the transpose of the inverse transform.

3. SYSTOLIC ARCHITECTURE FOR IMPLEMENTATION OF THE IDCT

Equation (15) may be expressed in a form $\mathbf{X}^T=\mathbf{D}\,[\mathbf{CY}]^T$ (16)

Where X and **Y** are matrices of size $N_1\times N_2$ while C and D are matrices of size $N_1\times N_2$and $N_2\times N_2$ respectively, which represent the transform kernels. For avoiding the transpose operation, equation (15) may otherwise be expressed as

$$X_{lm}=\sum_{J=0}^{N_2-1} Z_{lj}D_{mj} \quad (16a)$$

for

$$Z_{lj}=\sum_{i=0}^{N_1-1} C_{li}Y_{ij} \quad (16b)$$

where$l$= 0,1,..,$N_1$and m = 0,1,..,N_2-1

$$Y_{ij}=y(i,j) \quad (17)$$

$$C_{lj}=\cos\left[\frac{\pi(2l+1)i}{2N_1}\right] \quad (18)$$

$$D_{mj}=\cos\left[\frac{\pi(2m+1)j}{2N_2}\right] \quad (19)$$

As given by equation (16), the prime-factor IDCTmay be computed in two distinct stages. In the first stage, one has to perform multiplication of matrix [Y_{ij}] of size $N_1\times N_2$with N_1-point transform kernel [C_{lj}]of size $N_1\times N_1$to obtain an intermediate matrix [Z_{lj}] of size $N_1\times N_2$equation(16b). In the second stage, each row of intermediate matrix [Z_{lj}] is multiplied with the rows of N_2-point transform kernel [D_{mj}] of size $N_1\times N_2$, according to equation (16a). Multiplication of both these stages may be mapped into a systolic mesh containing $N_1\times N_2$PEs for fully pipelined processing. The proposed systolic structure for computing N-point transform, (N= $N_1\times N_2$), is shown in Fig. 1. The function of each PE is depicted in Fig.2. The first rows of the N_1-point transform kernel [C_{lj}] is fed of the first array. The successive rows of the transform kernels are fed to the successive arrays, staggered by one time-step with respect to the preceding one. The first column of the input matrix [Y_{ij}]is fed to the first PE of the first array. The successive columns are fed to the successive PEs of the first array in subsequent time-steps. The columns of the N_2-point transform kernel [D_{mj}] are fed to the different PEs of the first array at the lag of N_1 time-steps with respect to the corresponding columns of the input matrix [Y_{ij}]. In the first stage of computation, the (j+1)th PE of (l+1)th array computes an element [Z_{lj}] of the intermediate matrix in N_1 time-steps, where a PE performs a multiplication and adds the result to the content of the accumulator A_1, in every time-step. At the end of N_1 time-steps, the accumulator content is transferred to the accumulator A_2 while A_1 is reset to zero. In the second stage of computation, in each array, the multiplication of one row of the intermediate matrix [Z_{lj}] with N_2-point transform kernel [D_{mj}] is performed to obtainN_2 number of desired components.

4. HARDWARE AND THROUGHPUT CONSIDERATIONS

The systolic architecture for implementation of IDST as shown in Figure. 1 requires $N_1 \times N_2$ number of identical PEs. In each PE there are two multipliers, two adders and two accumulators.The

area complexity of the proposed structure is $O(N_1 \times N_2)$. The first transform component is obtained after $N_1 + N_2$time-steps. The first set of transform components is obtained after $2(N_1 + N_2 - 1)$time-steps. However, the successive sets of transform components are obtained in every N_2 time-step interval. The throughput rate of the proposed structure would, therefore, be $R = \left(\frac{N_1}{T}\right)$ where T is the duration of a time-step, given by $T = T_m + T_a$, T_m and T_a are, respectively, the time required for performing a real multiplication and a real addition in the PE. It is interesting to note that the transposition of the intermediate matrix is avoided in this structure by orthogonal processing during the pair of matrix multiplication i.e., if the processing for the first matrix multiplication takes place along X-direction, the processing for the second matrix multiplication is carried out along Y-direction. Due to this feature, the structure is highly compact, offers saving for transposition hardware and at the same time yields high throughput with less latency.

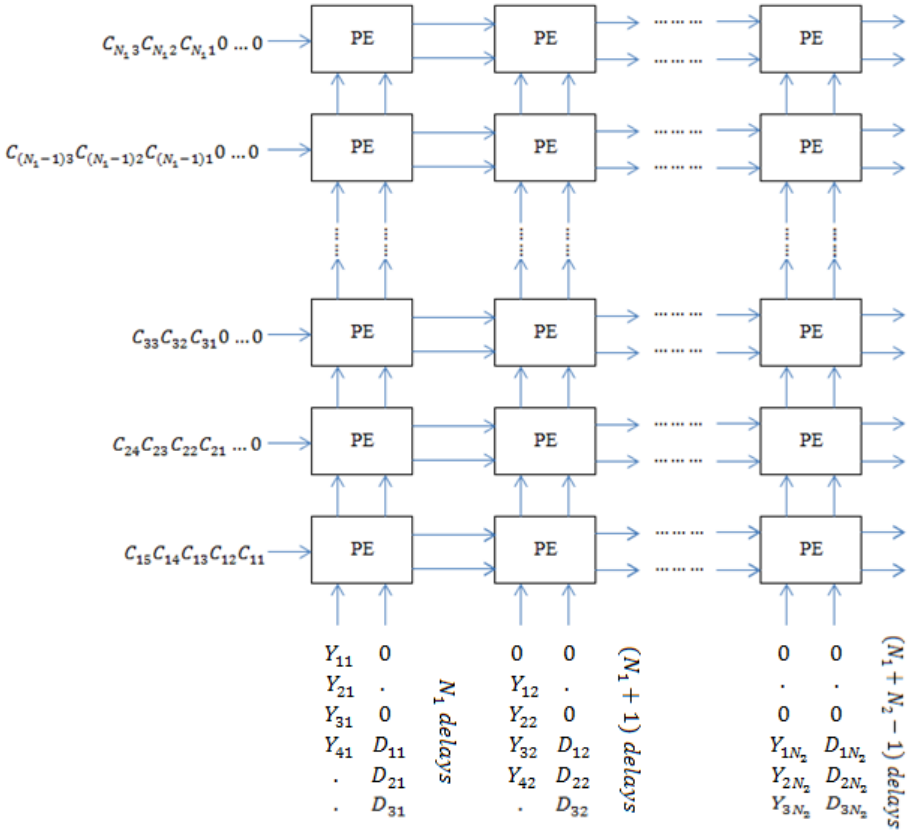

Figure 1. Systolic Architecture for Implementation of the IDST

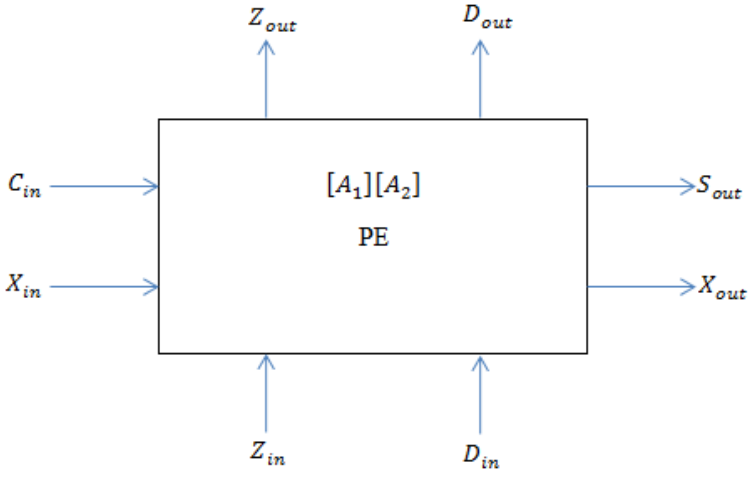

Figure 2.Function of each PE

Algorithm

1. $A_1 = A_2$
   $A_1 = 0$
2. $A_1 = A_i + C_{in}Z_{in}$
   $X_{out} = X_{in} + A_2D_{in}$
   $C_{out} = C_{in}$
   $D_{out} = D_{in}$
   $Z_{out} = Z_{in}$
   Count = Count + 1
   if (Count = N_1) go to 1
   else
   go to 2
   end if

TABLE 1 Comparison of Area Complexity, Computation Time and VLSI Performance Measure of the Structure for Computing Prime-factor IDCT of Size N × N.

Structures	Area Complexity (A)	Computation Time (τ)	VLSI Performance Measures ($A\tau^2$)
Structure of Lee and Huang [5]	$3N^2$	$3N$	$27N^4$
Structure of Gou et al. [3]	$(N^4 – 1)/2$	$(N^2 + 1)/2$	$(N^8 + 2N^6 - 2N^2 - 1)/8$
Systolic Architecture for IDCT (Figure 1)	N^2	$2N$	$4N^4$

5. Conclusion

We have suggested a simple scheme for prime-factor decomposition of IDCT and systolic mesh architecture for its implementation. It is interesting to note that the transposition of the intermediate matrix is avoided in this structure by orthogonal processing during the pair of matrix multiplication i.e., if the processing for the first matrix multiplication takes place along X-direction, the processing for the second matrix multiplication is carried out along Y-direction. Due to this feature, the structure is highly compact, offers saving for transposition hardware and at the same time yields high throughput with less latency.

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